
CMOS Single-Chip 8 bit Microcontroller with Vehicle Area Network (VAN) Data Link Controller

Description

The 80C51A30 is a stand alone high performances CMOS microcontroller designed for use in automotive and industrial applications.

The 80C51A30 retains all features of the MHS 80C51 with extended ROM capacity (16 K bytes), 256 bytes of RAM, a 7-sources 2-levels interrupt, a full duplex serial port, an on-chip oscillator and clock circuits, two 16 bits timers.

In addition, the 80C51A30 has an 8-bit 8-channel A/D converter, a serial peripheral interface compatible with SPI, an advanced 5 channel Event and Waveform Controller, a VAN network line controller and a 256 bytes extra RAM . A part of this RAM is used to store the VAN messages.

The VAN controller is fully compliant with the ISO standard ISO/11519-3. It implements all features of the 29C461 VAN data link controller, including a 256 bytes data dual port RAM.

The fully static design of the 80C51A30 allow to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The design is done with a specific care to reduce EMC emission and susceptibility.

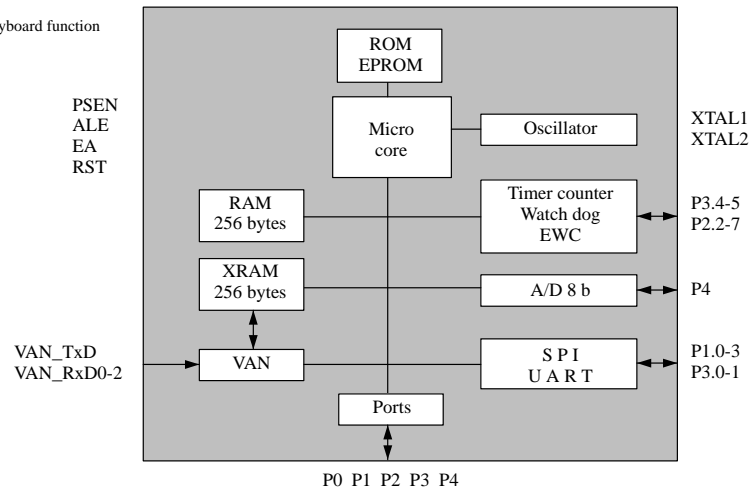
This circuit is manufactured using SCMOS process and is available in commercial, industrial, military and automotive ranges ; it runs from 0 up to 18 MHz in the automotive temperature range -40°C to $+125^{\circ}\text{C}$.

Features

- 80C51 core architecture
- 256 bytes of RAM, 256 bytes of XRAM
- 16 K bytes of ROM or OTP
- Four 8-bit I/O port
- Two 16 bit timer/counter
- A five channels Event and Waveform Controller with:
 - input capture
 - output compare and PWM
 - High security watchdog
 - Upward compatible with PCA
- A 8-bit resolution analog to digital converter with eight multiplex inputs
- One port with programmable interrupt for keyboard function
- Several power reduction modes with enhanced wake up capabilities
- Full duplex UART compatible with standard 80C51
- A serial peripheral interface (SPI)
- Full VAN controller
 - Fully Compliant with VAN standard ISO/11519-3.
 - 256 bytes DPRAM for received and transmitted messages (shared with XRAM)
 - 14 Identifier Registers with all bits individually maskable
 - 1 Mbits/s Maximum Transfer Rate
 - 3 Separate line inputs with automatic diagnosis and selection
 - Idle and Sleep modes
 - Manchester Enhanced or Impulsed Coding
- PQFP or PLCC 52 package

Block Diagram

Ports P0 with programmable interrupt for keyboard function



Pin Configuration

Pin PQFP52	Name	Function	Pin PQFP52	Name	Function
3	ANAVSS	Analog VSS	29	P2.3/A11/EWX0	Address bus high order or EWC module 0 external I/O
4	P4.0/ANA0/VCC1/2	Analog Input 0 or VCC / 2 output	30	P2.4/A12/EWX1	Address bus high order or EWC module 1 external I/O
5	P4.1/ANA1	Analog Input 1	31	P2.5/A13/EWX2	Address bus high order or EWC module 2 external I/O
6	P4.2/ANA2	Analog Input 2	32	P2.6/A14/EWX3	Address bus high order or EWC module 3 external I/O
7	P4.3/ANA3	Analog Input 3	33	P2.7/A15/EWX4	Address bus high order or EWC module 4 external I/O
8	P4.4/ANA4	Analog Input 4	34	PSEN	Program store enable
9	P4.5/ANA5	Analog Input 5	35	ALE/PROG	Address latch enable/Program pulse
10	P4.6/ANA6/REF+	Analog Input 6 or Analog positive reference	36	EA/VPP	External access enable/Programming supply voltage
11	P4.7/ANA7/REF-	Analog Input 7 or Analog negative reference	37	P0.7/AD7/KB0.7	Mux. low order address & data bus or Keyboard
12	ANAVCC	Analog VCC	38	P0.6/AD6/KB0.6	Mux. low order address & data bus or Keyboard
13	RST	Reset	39	P0.5/AD5/KB0.5	Mux. low order address & data bus or Keyboard
14	P3.0/RXD	Serial receive port	40	P0.4/AD4/KB0.4	Mux. low order address & data bus or Keyboard
15	P3.1/TXD	Serial transmit port	41	P0.3/AD3/KB0.3	Mux. low order address & data bus or Keyboard
16	P3.2/INT0	External interrupt 0	42	P0.2/AD2/KB0.2	Mux. low order address & data bus or Keyboard
17	P3.3/INT1	External interrupt 1	43	P0.1/AD1/KB0.1	Mux. low order address & data bus or Keyboard
18	XTAL2	Crystal output	44	P0.0/AD0/KB0.0	Mux. low order address & data bus or Keyboard
19	XTAL1	Crystal input	45	VSS	
20	VCC		46	VCC	
21	VSS		47	P1.0/MISO	SPI master in ,slave out
22	P3.4/T0	Timer/counter 0 input	48	P1.1/MOSI	SPI master out, slave in
23	P3.5/T1/CAN TX1	Timer/counter 1 input	49	P1.2/SCK	SPI serial clock I/O
24	P3.6/WR	External data memory write strobe	50	P1.3/SS	SPI slave select
25	P3.7/RD	External data memory read strobe	51	P1.4/VAN_RxD1	VAN receive RxD1
26	P2.0/A08	Address bus high order	52	P1.5/VAN_RxD2	VAN receive RxD2
27	P2.1/A09	Address bus high order	1	P1.6/VAN_RxD0	VAN receive RxD0
28	P2.2/A10/ECI	Address bus high order or EWC count input	2	P1.7/VAN_TxD	VAN transmit TxD

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